

# TDXdown: Single-Stepping and Instruction Counting Attacks against Intel TDX

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# Goal: Remove cloud provider from TCB



- AMD SEV-SNP
- Intel TDX
- (ARM CCA)







# Single-Stepping: The bane of TEEs





Interrupt Latency Attacks



Amplifier

Instruction Counting Attacks



Zero-Stepping Attacks

### History of Single-Stepping



# History of Single-Stepping



# History of Single-Stepping







Hypervisor



### Single-Stepping Countermeasure



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# Single-Stepping Attack









# StumbleStepping Attack







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- 3. Modular reduction approach:
  - 3.1 Sample candidate nonce k'
  - 3.2 Compute k as  $k' \mod n$



#### **Compute** $k' \mod n$



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#### Nonce Bias

#### Noncebit distribution given leaked loop iterations for secp160r1



#### StumbleStep Nonce Bias



#### Summary

- Primitive 1: full single-stepping
- Primitive 2: StumbleStepping; instruction counting
- Nonce truncation in wolfSSL and OpenSSL leaks for certain curves
- Responsible Disclosure:
  - Intel fixed primitive 1 with TDX module 1.5.06 but won't fix primitive 2
  - wolfSSL and OpenSSL switched to rejection sampling







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